Performances assessment of very high frequency class E inverters based on a load-oriented generic design method

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***Abstract*—Class E inverters are widely used in very high frequency power converters due to their ease-of-driving, their high efficiency and their low component count. A generic design method applicable to any load impedance, any output power (or input voltage) and any switching frequency is presented. The newly introduced visual tool is a support for designers to identify an optimal operating point. Depending on the application requirements, different operating point can be evaluated in terms of their performances. The method is carried out with three scenarii complying with the same requirements: 40.68 MHz, 50 W, and a 5 Ω Wireless Power Transfer load. The different designs are then compared and three prototypes are implemented and characterized to validate the method. The non-linear output capacitance of the GaN HEMT is entirely functionalized. The attained inverter efficiencies at the nominal operating point are measured between 87.7 % and 89.8 %.**

***Index Terms*—circuit design, class E, gallium nitride, power conversion, very high frequency, zero voltage switching**
[1]

I. Introduction

CLASS E inverters have attracted the attention of both academic and industrial researchers ([1], [2]) since their genesis in 1964 [3]. The motivation of their development was the achievement of very high efficiency (100 % theoretically) as a result of transistor current and voltage not overlapping (pure switching mode) and softly changing during the transitions (soft-switching) [1]. Since then, many researchers have contributed to the analysis and the design of class E inverters [1], [4], [5], [6], [7], [8]. More advanced considerations such as the effect of the ON-resistance [9], the finite quality factor of the output filter [5], the Finite DC-feed Inductor (FDI) [6], an arbitrary duty cycle [4], non-optimal switching conditions [10], [11] or a frequency multiplier with an output filter tuned to higher harmonics instead [6] have been studied deeply. Although largely employed in RF power amplification applications, the class E inverter has also been deployed in power conversion systems, such as DC to DC [2], [12], [13]. The advantages are the ease of driving and the high efficiency even at Very High Frequencies (VHF). One trend in power electronics systems is the increase of volumetric and gravimetric power density, in response to the systems being more and more electrified. Another research topic is the improvement of the power converters environmental footprint in regard for instance of the growing stress on primary resources [14]. The use of high frequency class E based power converters could lend some support to those challenges considering:

- Low component count
- Small passive components due to high switching frequencies
- Use of coreless (air-core) inductors due to low energy storage requirements
- Functionalization of parasitic elements such as the transistor output capacitance, leading to an even more reduced number of components

Class E inverters allowing a FDI and a switch driven with an arbitrary duty cycle are of particular interest for power conversion applications. Indeed, many possible designs exist due to more degrees of freedom and the dynamic response as well as the power density are enhanced since there is no bulky RF-choke. Reported design methods applied to such circuits are either analytical [8], [15] or numerical [16], [17]. The designer then faces the issue of identifying the best design for the considered application. To answer this question both approaches lack clarity, being either too complex or too costly. In this work, a graphical tool is introduced based on a class E inverter in-depth analysis. The presented design method is generic and can be applied to any set of output power (or input voltage), switching frequency and load impedance. A transistor with an arbitrary rated parasitic output capacitance (C_{oss}) can be chosen. The exploration of the design space allows to evaluate different operating points to compare their performance (efficiency, voltage and current stress, number of components, etc.). The method is direct as it doesn't require any further simulation tuning.

The work is carried out with the following outlooks in mind: class E inverters operating in the VHF range with a series LC filter, optimal switching conditions, a low number of components and an arbitrary load impedance. The design method is applied considering a load made of a resonant

[1] This paragraph of the first footnote will contain the date on which you submitted your paper for review, which is populated by IEEE.
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The graphical tool presented here is provided as supplementary material.
Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org

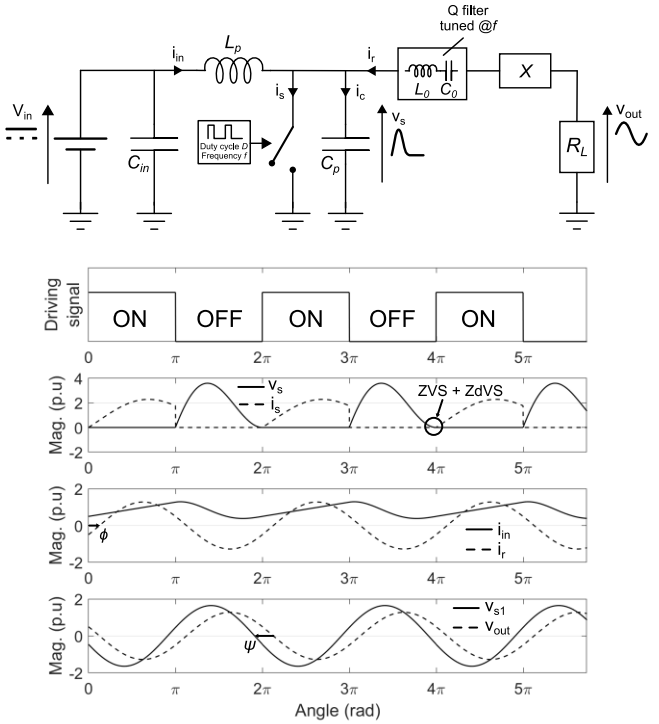


Fig. 1. Class E inverter electrical diagram and main waveforms (with q = 0.8 and D = 50 % in this case)

Wireless Power Transfer (WPT) system. A Gallium Nitride High Electron Mobility Transistor (GaN HEMT) that is suitable for high frequency power conversion due to low parasitic capacitances and low ON-resistance is chosen and air-core inductors (except for the RF-choke) are implemented.

The article is organized as follows. The class E inverter is first analyzed in Section II. From that, the design space is deeply explored in Section III, leading to the depiction of an appropriate operating area for power conversion systems. The proposed design method is then introduced in Section IV, carried out in Section V, and experimentally validated in Section VI. Finally, perspectives are discussed in Section VII.

II. The Class E Inverter

In this section, the analytical expressions describing the optimal behavior of the FDI class E inverter are presented. In order to encourage reproducibility, this section together with the appendix provide all the calculation steps needed to introduce the design method presented in section IV. More calculation steps can be found in [8], [18]. The analysis leads to a normalized circuit which is independent of the input voltage V_{in}, the resistive load R and the switching pulsation ω. The actual operating point is retrieved through a straightforward denormalization process presented in this section.

A. Electrical diagram and waveforms

Fig. 1 depicts the generalized circuit diagram of the class E inverter being analyzed. A square wave signal with an arbitrary ON duty cycle D and a frequency $f = \omega/2\pi$ drives the switch. In the method presented in this article, the design space is two-dimensional in regard with the two following parameters: the ON duty cycle D and the ratio $q = 1/\omega\sqrt{L_pC_p}$ between the input network $L_p - C_p$ resonant frequency and the switching frequency f. In the case of RF-choke (conventional) class E circuits this ratio tends to 0.

The main normalized waveforms with an input voltage V_{in} equal to 1, a resistive load R_L equal to 1 Ω and a switching pulsation ω equal to 1 rad.s^{-1} for a certain operating point ($q = 0.8$ and $D = 50$ %) are shown in **Fig. 1**. The typical class E voltage waveform appears across the switch when it is open, as a result of the charge/discharge of the shunt capacitance C_p. Input inductance L_p and series reactance X help to discharge C_p in order to achieve the so-called optimal switching conditions just before the switch turns on (Zero Voltage Switching ZVS and Zero Derivative Voltage Switching ZdVS shown in **Fig. 1**). The series $L_0 - C_0$ filters out DC and high order harmonics such that a pure AC voltage is generated across the resistive load R_L. The quality factor is defined as $Q = L_0\omega/R_L$. Angles ϕ and ψ are defined as follows: ϕ is the initial phase shift of the current i_r relative to the switch turn-on (negative in **Fig. 1**), and ψ is the phase shift of the first harmonic component v_{s1} of v_s with respect to the output voltage v_{out} (positive in **Fig. 1**).

When optimal switching conditions are met, all parameters of the normalized circuit are only dependent onto q and D and their closed-form expressions are known, as is shown thereafter. The normalized current and voltage waveforms and the normalized transmitted power are only $\{q, D\}$-dependent as well. The exploration of the 2D design space is then made possible, which is a considerable advantage of this analytical method. Appropriate operating area (including various operating points $\{q; D\}$) are then identified based on power electronics designer-oriented criteria, as shown in section III.

B. Circuit analysis

1) **Design assumptions**

The analysis is based on the following assumptions:

- Transistor is ideal (no power losses and instantaneous switching)
- Passive components are ideal (no power losses)
- Output capacitance of the transistor is linear (constant)
- Input voltage is constant
- Current i_r is sinusoidal at the switching frequency

2) **Time-domain analysis**

As assumed, the high-Q LC filter in the output branch leads to a current i_r defined as:

$$i_r(\theta) = I_r\sin(\theta + \phi) \quad (1)$$

with $\theta = \omega t$ and I_r the magnitude. The output voltage v_{out} is then given by:

$$v_{out(\theta)} = -R_L I_r\sin(\theta + \phi) \quad (2)$$

When the switch is *ON* ($0 < \theta < 2\pi D$) C_p is bypassed ($v_s = 0$) and the input voltage source linearly charges L_p. The expression of i_{in} reads:

$$i_{in}(\theta) = I_r(\theta/p - \sin(\phi)) \quad (3)$$

Where the normalized parameter:

$$p = L_p\omega I_r/V_{in} \quad (4)$$

is introduced for the rest of the analysis. The expression of the switch current $i_s = i_{in} + i_r$ immediately follows:

$$i_s(\theta) = I_r(\theta/p + \sin(\theta+\phi) - \sin(\phi)) \quad (5)$$

When the switch is *OFF* ($2\pi D < \theta < 2\pi$) a first analysis of the circuit leads to the following 2nd order ODE:

$$L_p C_p \omega^2 \frac{d^2 v_s(\theta)}{d\theta^2} + v_s(\theta) = V_{in}(1 + p\cos(\theta+\phi)) \quad (6)$$

Solving (6) for $v_s(\theta)$ gives:

$$\frac{v_s(\theta)}{V_{in}} = 1 + k_1\cos(q\theta) + k_2\sin(q\theta) + \frac{q^2 p}{q^2-1}\cos(\theta+\phi) \quad (7)$$

Where parameters k_1 and k_2 are two constant parameters. The i_c expression is derived from (7) and rearranged with (4):

$$i_c(\theta) = \frac{I_r}{qp}\left(-k_1\sin(q\theta) + k_2\cos(q\theta) - \frac{qp}{q^2-1}\sin(\theta+\phi)\right) \quad (8)$$

Following (1) and (8), $i_{in} = i_c - i_r$ is written as:

$$i_{in}(\theta) = \frac{I_r}{qp}\left(-k_1\sin(q\theta) + k_2\cos(q\theta) - \frac{q^3 p}{q^2-1}\sin(\theta+\phi)\right) \quad (9)$$

Two continuity equations:

- Voltage across C_p: $v_s(2\pi D^+) = v_s(2\pi D^-) = 0$
- Current in inductors: $i_c(2\pi D^+) = i_s(2\pi D^-)$

and two boundary conditions:

- ZVS: $v_s(2\pi) = 0$
- ZdVS: $dv_s(\theta = 2\pi)/d\theta = 0$

are applied onto the expression of v_s in the *OFF* state (7) and onto the expression of the currents (5) and (8). Those equations yield to $\{q, D\}$-dependent expressions for the parameters k_1, k_2, ϕ and p that are given in the appendix.

3) **Parameter g_x**

The parameter g_x defined as:

$$g_x = < i_s >_{2\pi}/I_r = I_{in}/I_r \quad (10)$$

where I_{in} is the DC (average value) input current, is $\{q, D\}$-dependent only and its expression is given in the appendix. It allows the circuit parameters to be written in a compact form.

4) **First Harmonic Approximation (FHA)**

It is assumed that full part of the power is transmitted to the load at first harmonic due to the output LC filter. The first harmonic component of v_s is analytically derived:

$$v_{s1}(\theta) = V_{in}(V_R\sin(\theta+\phi) + V_X\cos(\theta+\phi)) \quad (11)$$

The $\{q, D\}$-dependent expressions of the coefficients V_R and V_X are derived with Fourier series analysis and are given in the appendix. The excess reactance X is then calculated as:

$$X = \frac{V_X}{V_R}\cdot R_L \quad (12)$$

And the angle ψ is calculated as:

$$\psi = \operatorname{atan}\left(\frac{V_X}{V_R}\right) \quad (13)$$

5) **Circuit parameters**

The input power P is assumed to be entirely transmitted to the load:

$$P = V_{in}I_{in} = R_L I_r^2/2 \quad (14)$$

Exploiting the definitions of the parameters p, g_x and P, the following expression is derived:

$$p = \frac{L_p\omega I_r}{V_{in}}\cdot\frac{2R_L I_r g_x}{2R_L I_{in}} = 2g_x\frac{L_p\omega}{R_L} \quad (15)$$

And resulting from (10) and (15), the circuit parameters can be retrieved:

$$L_p = \frac{p}{2g_x}\cdot\frac{R_L}{\omega} \quad (16)$$

$$C_p = \frac{1}{q^2\omega^2 L_p} = \frac{2g_x}{q^2 p}\cdot\frac{1}{R_L\omega} \quad (17)$$

$$I_r = 2g_x\cdot\frac{V_{in}}{R_L} \quad (18)$$

$$P = 2g_x^2\cdot\frac{V_{in}^2}{R_L} \quad (19)$$

$$R_{DC} = \frac{V_{in}}{I_{in}} = \frac{1}{2g_x^2}\cdot R_L \quad (20)$$

where R_{DC} is the DC resistance seen by the voltage source.

6) **Normalization**

As highlighted in expressions (16)-(20), the circuit parameters can be normalized with respect to the input voltage, the resistive load and the switching pulsation. Normalized parameters as well as normalized waveforms are marked in the rest of the article with a tilde symbol. In order to retrieve the actual operating point, the denormalization is performed considering the actual input voltage V_{in}, load R_L and switching pulsation ω. TABLE I summarizes the normalization considered in the analysis depending on the nature of the parameter.

TABLE I
NORMALIZATION WITH RESPECT TO V_{in}, R_L AND ω

Parameter	Normalization (p. u.)
Resistance	$\tilde{R} = R\cdot\frac{1}{R_L}$
Reactance	$\tilde{X} = X\cdot\frac{1}{R_L}$
Current (waveform or magnitude)	$\tilde{\imath} = i\cdot\frac{R_L}{V_{in}}$
Voltage (waveform or magnitude)	$\tilde{v} = v\cdot\frac{1}{V_{in}}$
Power	$\tilde{P} = P\cdot\frac{R_L}{V_{in}^2}$

Some papers [8] [10] [11] refer to the "design set" $\{K_X, K_L, K_C, K_P\}$ which is retrieved in the normalized expressions of parameters $\tilde{X}$(12), $\tilde{L}_p$(16), $\tilde{C}_p$(17) and $\tilde{P}$(19). From that point and for the rest of the analysis, calculations are directly made with respect to the normalized circuit.

7) **Constraints on the switch**

The peak switch voltage in the class E topology reaches relatively high value (e.g 3.56 times the input voltage for a RF-choke class E inverter operating at 50% duty cycle [1]). This constraint can rise to even larger values for high value of D. As the theoretical peak switch voltage V_{sp} can only be obtained numerically, the authors in [19] provide a fitted expression in terms of q and D of the normalized V_{sp} attained across the switch, which reads:

$$\tilde{V}_{sp} = \frac{1.7613 + 0.05q}{1-D} \quad (21)$$

The capacitance C_p is partly brought by the inherent C_{oss} of the switch, and in high frequency implementations the C_{oss}

could even constitutes the whole C_p. Due to the non-linearity of C_{oss}, V_{sp} reaches even higher values (a safe margin of 20 % overvoltage can be taken as a rule of thumb [20] then it is considered in this work).

Regarding the peak current I_{sp} in the switch, it is useful to derive its analytic expression, since it permits to estimate theoretically the value of the power output capability c_p commonly evaluated in the design of power amplifiers. This parameter estimates the normalized "utilization" of the switch in terms of current and voltage, hence its definition:

$$c_p = \frac{P}{V_{sp} I_{sp}} \tag{22}$$

The expression (22) holds with the normalization:

$$c_p = \frac{\tilde{P}}{\tilde{V}_{sp} \tilde{I}_{sp}} \tag{23}$$

$\tilde{I}_{sp}$ is the maximal value attained by $\tilde{\imath}_s(\theta)$. Two cases are to be considered:

Case 1: $\tilde{I}_{sp}$ is the value taken by $\tilde{\imath}_s$ at turn-on (5):

$$\tilde{\imath}_s(2\pi D) = \frac{2g_x}{p}\left(2\pi D + \frac{\sin(2\pi D + \phi) - \sin(\phi)}{p}\right) \tag{24}$$

Case 2: $\tilde{I}_{sp}$ is the value taken by $\tilde{\imath}_s$ (5) at the instant of zero derivative:

$$\frac{d\tilde{\imath}_s(\theta)}{d\theta} = 0 \;\rightarrow\; \theta_p = \operatorname{acos}\left(-\frac{1}{p}\right) - \phi \tag{25}$$

Case 2 is not defined when $p < 1$, then *case* 1 is considered. If $\theta_p > 2\pi D$, *case 1* is considered as well. Finally, $\tilde{I}_{sp}$ obtained with both *cases* needs to be compared and the largest value kept. **Fig. 2** shows the different trends of the switch current and which case has to be considered to estimate theoretically $\tilde{I}_{sp}$.

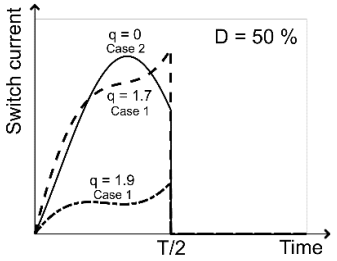


Fig. 2. Switch current shape with different values for q

8) **Power losses in the inductors**

Due to skin and proximity effects in inductors becoming an issue at high frequencies, it is interesting to define two figures of merits for the resistive losses in inductors L_0 and L_p. These losses depend on the Equivalent Series Resistance (ESR) which is frequency-dependent. The ESR can be generally written in terms of the inherent quality factor Q_{ind} of the inductor which is usually specified by the manufacturer for a given frequency:

$$ESR = \frac{L\omega}{Q_{ind}} \tag{26}$$

Losses in the inductor L_0 are then expressed as:

$$P_{L0} = \frac{ESR_{L0} \cdot I_r^2}{2} = \frac{L_0 \omega I_r^2}{2Q_{ind_{L0}}} \tag{27}$$

And by combining (18), (27) and the definition of Q:

$$P_{L0} = \frac{2g_x^2 Q}{Q_{ind_{L0}}} \cdot \frac{V_{in}^2}{R_L} \tag{28}$$

The normalized losses $\tilde{P}_{L0}$ directly reads from (28):

$$\tilde{P}_{L0} = \frac{2g_x^2 Q}{Q_{ind_{L0}}} \tag{29}$$

And with respect to the normalized power $\tilde{P}$ a figure of merit ρ_{L0} can be defined from (29):

$$\rho_{L0} = \frac{\tilde{P}_{L0}}{\tilde{P}} = \frac{Q}{Q_{ind_{L0}}} \tag{30}$$

As expected, a trade-off has to be considered for Q. High Q values lead to purer sinusoidal current flowing into the load (and design assumptions more valid). On the other hand, this leads to higher resistive losses in the filter, considering a roughly constant $Q_{ind_{L0}}$. The resistive losses in L_p can be estimated with the AC content $I_{inAC} = \sqrt{I_{inRMS}^2 - I_{in}^2}$ of the input current because DC-resistance is typically at least one order of magnitude lower than the ESR at switching frequency. As a first approximation, the ESR value at the switching frequency is considered, hence the expression:

$$P_{Lp} = ESR_{Lp} \cdot I_{inAC}^2 = \frac{L_p \omega I_{inAC}^2}{Q_{ind_{Lp}}} \tag{31}$$

In terms of the normalized current $\tilde{I}_{inAC}$ whose expression is given in the appendix, P_{Lp} reads:

$$P_{Lp} = \frac{L_p \omega \tilde{I}_{inAC}^2}{Q_{ind_{Lp}}} \cdot \left(\frac{V_{in}}{R_L}\right)^2 \tag{32}$$

And by combining (16) and (32), the normalized losses $\tilde{P}_{Lp}$ are obtained:

$$P_{Lp} = \frac{p\tilde{I}_{inAC}^2}{2g_x Q_{ind_{Lp}}} \tag{33}$$

As for the losses in the filter inductor, a figure of merit for the losses in L_p relatively to the output power can be defined:

$$\rho_{Lp} = \frac{\tilde{P}_{Lp}}{\tilde{P}} = \frac{p\tilde{I}_{inAC}^2}{4g_x^3 Q_{ind_{Lp}}} \tag{34}$$

Both figures of merit are explored in Section III. All the class E inverter normalized circuit parameters are gathered in the TABLE V provided in the appendix.

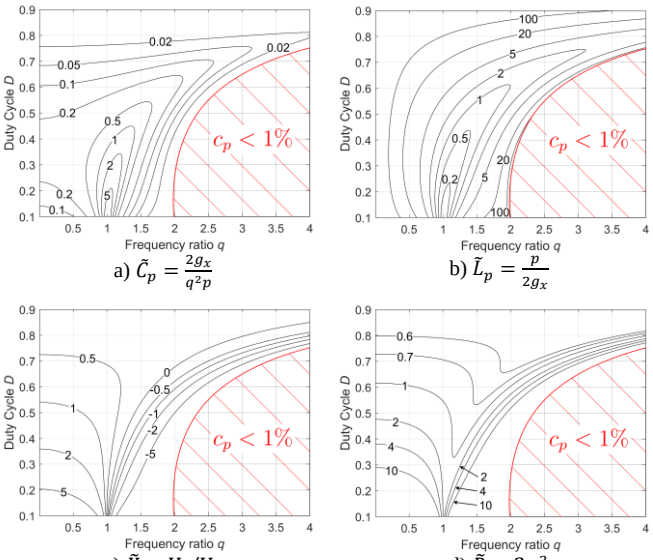
III. Exploration of the 2-dimensional design space

The analysis conducted in Section II is exploited here. The 2D design space is explored varying q and D in order to draw conclusions regarding the operating area of interest. The operating points leading to power output capability c_p lower than 1 % are disregarded due to poor interest for power electronics applications.

A. Normalized parameters in the 2D design space

The evolution of the electrical parameters $\tilde{C}_p$, $\tilde{L}_p$, $\tilde{X}$ and $\tilde{P}$ in the design space are shown in **Fig. 3**. In **Fig. 3** a) there is an area (around $q = 1$ and for low duty cycle) with high $\tilde{C}_p$. This points out the ability for the FDI class E inverter to operate with high C_p for given R_L and ω, allowing the use of transistors with

higher C_{OSS} value. In this same area, the normalized inductance is low as revealed in **Fig. 3** b). The current ripple is enlarged consequently and this should be considered. The curve for $\tilde{X} = 0$ in **Fig. 3** c) corresponds to the "parallel class E amplifier" circuit described in [20] which maximizes the output power. As shown in **Fig. 3** d) the normalized power increases with the duty cycle as well as in the vicinity of the curve where $\tilde{X} = 0$. The normalized input DC resistance is equal to the inverse of $\tilde{P}$.

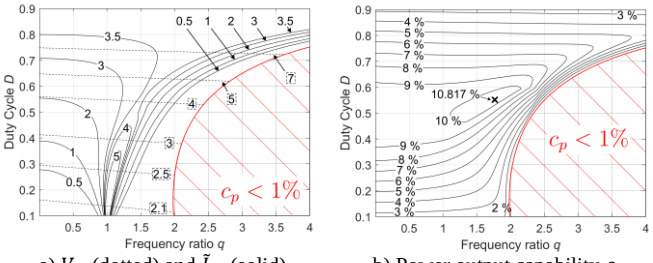


a) $\tilde{C}_p = \frac{2g_x}{q^2 p}$ b) $\tilde{L}_p = \frac{p}{2g_x}$

c) $\tilde{X} = V_X/V_R$ d) $\tilde{P} = 2g_x^2$

Fig. 3. Exploration of parameters $\tilde{C}_p$, $\tilde{L}_p$, $\tilde{X}$ and $\tilde{P}$

Fig. 4 depicts the evolution of the switch constraints as well as the power output capability c_p. From **Fig. 4** a), the normalized voltage stress primarily depends on the duty ratio whereas the normalized peak current intensifies around $q = 1$. A general observation from **Fig. 4** b) is the increase of c_p around the duty cycle of 50 %. The power output capability c_p for a class E inverter reaches a maximum value of about 10.8 % for $D = 55$ % and $q = 1.77$. Moreover, The c_p values for $q = 0$ (conventional) agree with [21].



a) V_{sp} (dotted) and $\tilde{I}_{sp}$ (solid) b) Power output capability c_p

Fig. 4. Exploration of voltage/current constraints on the switch

To estimate the evolution of the relative losses ρ_{Lp} and ρ_{L0} in the inductors, a quality factor Q_{ind} value has to be considered. In this section a value of 200 is chosen, which is not conservative in order to not restrain too much the operating area. Air-core high-current flat wire solenoids from Coilcraft can reach this value [22]. Designers can still adjust this value with respect to their actual specifications. Regarding the inductor L_0, the impact of a variation of the loaded Q factor has to be assessed since the relative losses depends on it (29). For that purpose, an exploration in simulation (with ideal component models) is carried out. As expected, lower values of Q take us away from the design assumptions, meaning optimal switching conditions are likely lost as illustrated in **Fig. 5**. Two deviations may appear and are defined as:

$$\text{Loss of ZVS: } v_s(2\pi)/V_{sp} \tag{35}$$

$$\text{Inverse conduction ratio: } V_{sm}/V_{sp} \cdot T_{inv}/T \tag{36}$$

The former leads to EMI issues and to an increase of the switching losses and the latter to an increase of power losses due to poor inverse conduction performances of the GaN HEMT. It is considered in this work that both criteria should not exceed 5 %.

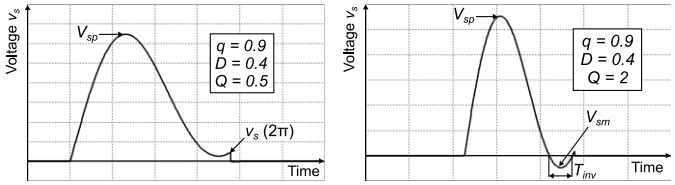
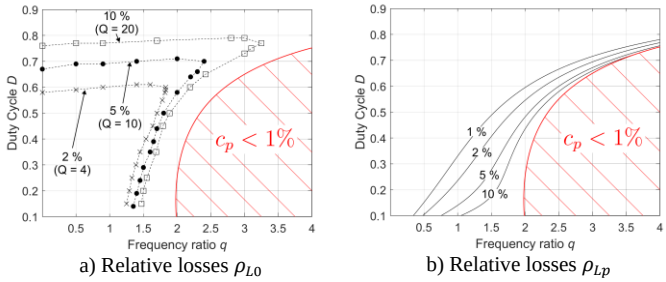


Fig. 5. Two criteria are identified in simulation: the loss of the ZVS (left) and the inverse conduction (right)

Different limits in the 2D design space are drawn from this explorative simulation and the two criteria previously defined. Regarding the input inductor, the losses can be analytically derived from (34). The evolution of both relative losses in the inductors is represented in **Fig. 6**. The ones occurring in L_0 are essentially increased for wider duty cycles due to large required Q factor (**Fig. 6** a), whereas the relative losses in L_p mostly restrict the area with large q and low duty cycle (**Fig. 6** a).



a) Relative losses ρ_{L0} b) Relative losses ρ_{Lp}

Fig. 6. Normalized relative losses in inductors L_0 and L_p

B. Identification of the appropriate operating area

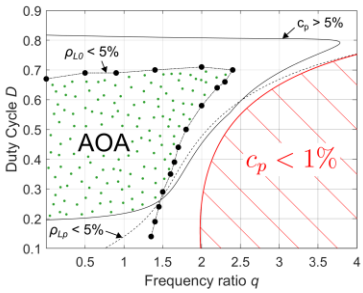


Fig. 7. Illustration of the appropriate operating area (AOA)

In regard with the following power conversion-oriented criteria on the parameters c_p, ρ_{Lp} and ρ_{L0}:

- $c_p > 5$ % (see **Fig. 4** b)
- $\rho_{Lp} < 5$ % (see **Fig. 6** a)
- $\rho_{L0} < 5$ % (see **Fig. 6** b)

An appropriate operating area (AOA) for the design of class E inverter is identified and dotted in **Fig. 7**. This constitutes the design space boundaries for the rest of the article. Designers can still adjust those parameters limits to their needs and even add other criteria such as the input inductance value.

IV. Design Method

The objective of this section is to introduce a straightforward design method based on the exploitation of the 2D analytical design space. With the same specifications, several designs can be developed as will be shown thereafter.

A. Specifications

The following specifications are considered for the class E inverter design method: the switching frequency f, the output power P, the transistor (and its corresponding non-linear C_{OSS}) and the load impedance $Z_L = R_L + jX_L$. Optimal switching conditions are to be met as well. Capacitance C_p can be partially or entirely brought by the transistor C_{OSS}, as shown on the electrical diagram in **Fig. 8**. This latter is non-linear and distortion occurs in the v_s waveform. It is often preferred to add an external capacitor to linearize the circuit behavior in the OFF-state and reduce losses [23]. On the other hand, stray inductance is inevitably added with it, leading to even higher frequency voltage oscillations on the drain node. In this work, the default choice is to only use the transistor C_{OSS} which lowers the component count and mitigates drain node voltage oscillations. This is generally feasible in the VHF range considering the low required C_p (less than 1 nF). If no appropriate operating point exists, an external capacitance C_{p-ext} can still be added. Another degree of freedom is the addition of a matching reactance X_m (either positive or negative) in series in the output branch. A matching network [24] could be used to modify the load impedance if no operating point has been found. This last option is not considered here.

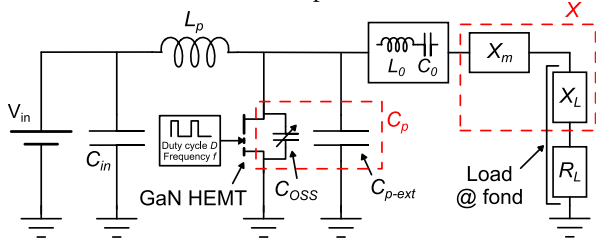


Fig. 8. Electrical diagram of the class E inverter considered in the design method (see **Fig. 1** for comparison)

The time-related output capacitance $C_{O_{TR}}$ is defined as:

$$C_{O_{TR}}(v_s) = \frac{Q_{OSS}}{v_s} = \frac{\int_0^{v_s} C_{OSS}(v_s^*)dv_s^*}{v_s} \tag{37}$$

It is a linear equivalent capacitor in substitute of the actual transistor output capacitance, that gives the same charging time as the non-linear capacitance for a given charging current. The expression of the voltage-dependent C_{OSS} is usually provided in the manufacturers models or can be extracted from DC-biased HF measurements [25]. $C_{O_{TR}}(V_{sp})$ is chosen in the method to account for C_p, hence the maximum drain voltage V_{sp} has to be known. The theoretical input voltage V_{in} needed to ensure a certain power level P is calculated as:

$$V_{in} = \sqrt{R_L P/\tilde{P}} \tag{38}$$

V_{sp} is then estimated using (21). The method is iterative because V_{sp} influences the design. The higher-than-expected peak voltage induced by the non-linearity of the C_{OSS} is neglected in the calculation of $C_{O_{TR}}(V_{sp})$.

B. Design process

The designer is facing a question: "Does it exist an operating point $\{q, D\}$ in the 2D normalized design space complying with the requirements, and are there circuit modifications (addition of C_{p-ext} or X_m) to make?". In order to rapidly provide an answer, a decision support tool in the form of a chart is developed. The method describes a "load-based" approach, where the load impedance is a starting point of the process. This approach is suitable for the design of VHF power converters since the load is usually not standardized, and even for DC-DC converters where the rectifier impedance is an input to the design of the inverter [2], [12]. For WPT systems (as studied in this work) the impedance seen at the primary side can be a specification as well. The two parameters r and x (39)-(40) are then introduced and plotted in a chart (see **Fig. 9**):

$$r = R_L C_p \omega \tag{39}$$

$$x = X C_p \omega \tag{40}$$

Where X is the reactance of the output branch at the switching frequency (equals to $X_L + X_m$, see **Fig. 8**). The objective is then to find an intersection point of the r and x isolines. High quality copy of the chart is provided as supplementary material for reproducibility. The design process is summarized in a schematic view in **Fig. 10**.

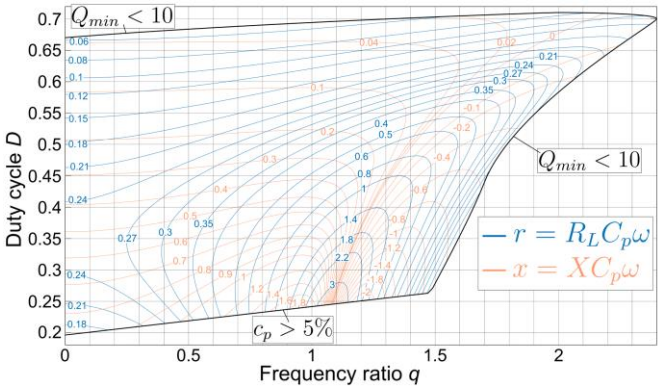


Fig. 9. Parameters r and x plotted in the 2-dimensional space

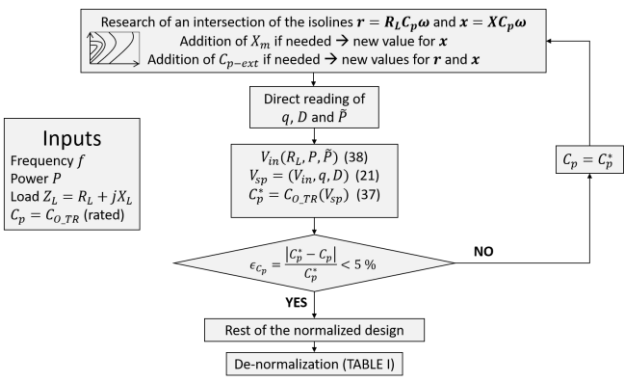


Fig. 10. Design method: inputs and design process

V. Examples: three 40.68 MHz FDI class E inverters

The method is applied to the design of three 40.68 MHz class E inverters supplying power to a WPT system made of two Printed Circuit Board (PCB) resonant coils (**Fig. 11**). This WPT resonant load is functionalized to replace the L_0 - C_0 filter in **Fig. 8** (it inherently filters out DC and harmonics) as well as the parasitic output capacitance C_{OSS} of the transistor.

A. The WPT system

Two resonant coils are built and both series-compensated with a 68-pF multi-layer ceramic capacitor in order to appear resistive at 40.68 MHz (based on the work in [26]). The resistance seen from the primary side depends strongly on the distance between the two PCB coils. With a 10 Ω load connected to the secondary side and a distance of $d = 2.5$ cm, the measured impedance is equal to $Z_L = 5\Omega + \mathrm{j}0\Omega$, as shown in **Fig. 11**.

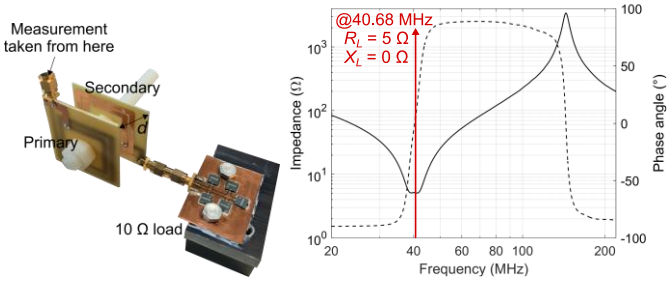


Fig. 11. Photograph of the WPT load (left) and measured impedance magnitude (solid) and angle (dotted) (right)

B. Comparison between the three scenarii

The following specifications are considered: a 40.68 MHz switching frequency, a power of 50 W, the 5 Ω WPT load and the GaN HEMT GS61004B® (100 V, 38 A, 16 mΩ) which has a rated C_{O_TR} of 180 pF for $v_s = 50\,V$. The v_s-dependence of C_{OSS} is provided in the manufacturer spice model and $C_{O\_TR}(V_{sp})$ can be calculated using (37). Parameters r and x are calculated using (39)-(40): $r = 0.23$ and $x = 0$. The design method presented in Section IV is applied in regard with these specifications, and three scenarii are considered leading to three different operating points in the $\{q, D\}$ design space. The first scenario gives a straightforward operating point without any modifications to the circuit. The second one considers a RF-choke ($q = 0$) as input inductor using a matching reactance X_m. The third one attains a load-independent operating point ($q = 1.29$ and $D = 0.5$ as mentioned by authors in [27]) thanks to a reactance X_m and an additional C_{p_ext}. The design method is applied and resulting operating points are given in TABLE II as well as the de-normalized circuit parameters.

The three operating points are all verified to be within the AOA. Besides, two other constraints need to be verified. In regard with the blocking voltage of the GaN HEMT and the 20 % safety margin due to the non-linearity of the C_{OSS}, a maximum peak voltage V_{sp} of 80 V is allowed. Since this work wants to demonstrate the effectiveness of the design method, aspects relative to transistor lifetime and reliability are beyond its scope, hence the maximum drain voltage close to the transistor blocking voltage. V_{sp} is estimated using (21) and (38). Considering the available high current air-core inductors in the market, a minimal value of 20 nH has been chosen. With respect to a 5 Ω load and a 40.68 MHz switching frequency, the normalized $\tilde{L}_p$ has to be above 1.02 (16). As can be seen in **Fig. 12**, the three chosen operating points are within areas where those two constraints are respected.

TABLE II
Design method results for the three scenarii

	Scenario 1	Scenario 2	Scenario 3
Supp. constraints	No	$q = 0$	$q = 1.29$ $D = 0.5$
Number of it.	1 ($\epsilon_{Cp} = 0.6$ %)	1 ($\epsilon_{Cp} = 3.1$ %)	0
Operating point	$q = 1.78$ $D = 0.63$	$q = 0$ $D = 0.47$	$q = 1.29$ $D = 0.5$
Parameters r and x	$r = 0.22$ $x = 0$	$r = 0.21$ $x = 0.26$	$r = 1$ $x = 0.15$
Circuit parameters	$\tilde{X} = 0$ $\tilde{P} = 1.62$ $\tilde{L}_p = 1.46$	$\tilde{X} = 1.28$ $\tilde{P} = 0.48$ $\tilde{L}_p = \infty$	$\tilde{X} = 0.28$ $\tilde{P} = 1.26$ $\tilde{L}_p = 1.04$
De-normalized parameters	$V_{in} = 12.5\,V$ $V_{sp} = 62.5\,V$ $L_p = 28.6\,nH$ $C_p = 169\,pF$	$V_{in} = 22.5\,V$ $V_{sp} = 75\,V$ $L_p > 3\,\mu F$ ($\Delta i_{in} < 5$ %) $C_p = 161\,pF$ $L_m = 25.1\,nH$	$V_{in} = 14\,V$ $V_{sp} = 51\,V$ $L_p = 20.4\,nH$ $C_p = 451\,pF$ $C_{p\_ext} = 271\,pF$ $L_m = 5.5\,nH$

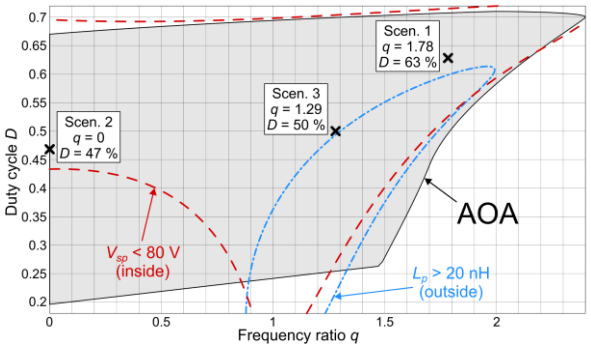


Fig. 12. The three operating points locations in the restricted AOA considering the constraints: $V_{sp} < 80\,V$ and $L_p > 20\,nH$

Optimal switching conditions were observed for each scenario and there was no need for further optimization by tuning the parameters. The expected pros and cons of the scenarii are summarized in TABLE III.

TABLE III
Pros and cons for each scenario

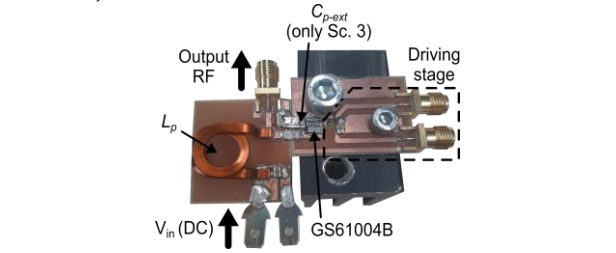
	Advantages	Disadvantages
Scenario 1	Less components No RF-choke	Switch voltage stress Input current ripple
Scenario 2	Constant input current	Bulky RF-choke Switch voltage stress
Scenario 3	No RF-choke Lower switch voltage stress Load-independent	External shunt cap. Input current ripple

VI. Experimental validation

A. The prototypes

Three prototypes of class E inverters corresponding to the three scenarii described in Section V are implemented. The

components values are given in TABLE IV. The gate driver LMG1020 from Texas Instrument drives the GaN HEMT with 0-5 V pulses at the duty cycle D. The pulse signal is supplied by the arbitrary waveform generator Tektronix AFG 3252. A single main board for the GaN HEMT and the driving stage is built. Depending on the scenario, a different board holding the rest of the passive components is soldered to this board, as shown in the photographs of **Fig. 13** where the board corresponding to the first scenario is soldered to the main board for example. The WPT load is connected as close as possible to the output RF port. The objective of these three prototypes is to validate the design method; hence no layout optimization was carried out. The major impact of this is the degradation of the output power, caused by the parasitic inductance in series with the switch, as will be shown in the Discussion.



a) Scen. 1 board (28 x 48 mm) with the main board (40 x 44 mm)

b) Scen. 2 board (16 x 56 mm) c) Scen. 3 board (16 x 52 mm)

Fig. 13. Photographs of the three class E inverter prototypes

TABLE IV
PASSIVE COMPONENTS CHOSEN FOR EACH SCENARIO

	Scenario 1	**Scenario 2**	**Scenario 3**
L_p	33 nH (2014VS-33N)	3.3 µH (MSS1048-332N)	22 nH (1212VS-22N)
C_{p_ext}	N.A.	N.A.	220 pF NP0 500V + 47 pF NP0 500V
L_m	N.A.	22 nH (1212VS-22N)	10 mm long microstrip

B. Experimental waveforms

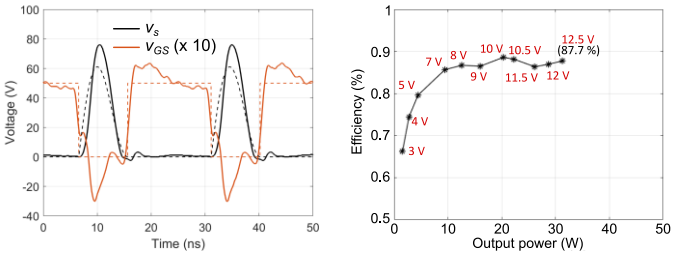
Drain source voltage v_s and gate source voltage v_{GS} where measured with the passive voltage probe Probe Master 500 MHz 5905-1RA connected to the Tektronix MSO64 scope. The obtained results are given in **Fig. 14** for each scenario. The efficiency is estimated for the inverter part (without the L_0 - C_0 filter part brought by the load itself) as:

$$\eta = \frac{P_{outRF}}{P_{inDC} + P_{drive}} \tag{41}$$

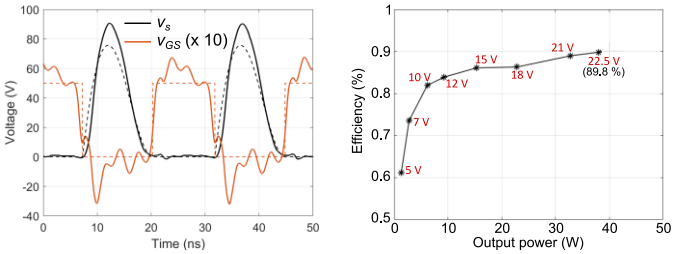
Where the input power P_{inDC} as well as the driving power P_{drive} are directly obtained using DC measurements. The output power P_{outRF} is estimated by measuring the output voltage (just before the WPT load) and by summing each harmonic contribution:

$$P_{outRF} = \sum_{i=1}^{\infty} \frac{{V_{out_i}}^2 R_i}{2(R_i + X_i)^2} \tag{42}$$

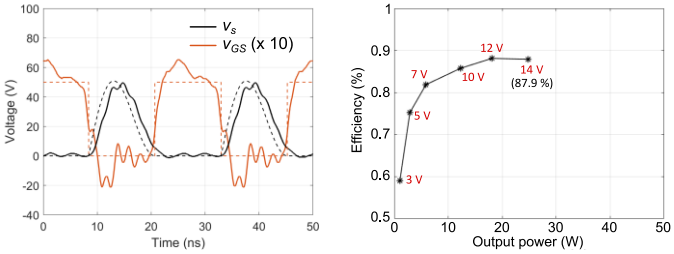
Where R_i and X_i are the real and imaginary parts of the WPT load impedance (given in terms of module and phase in **Fig. 11**) and V_{out_i} the magnitude of the measured output voltage at ith-harmonic. In practice, only the five first harmonics are considered.



a) Scenario 1 ($q = 1.78$, $D = 0.63$)



b) Scenario 1 ($q = 0$, $D = 0.47$)



c) Scenario 1 ($q = 1.29$, $D = 0.5$)

Fig. 14. v_s and v_{GS} waveforms (theoretical in dashed line – measured in solid line) and measured efficiency

The optimal switching conditions are attained for each scenario which validates the design method. The measured inverter efficiency is consistent with existing works in the literature [2], [12]. The transistor temperature measured with thermal imaging reaches respectively 73 °C, 64 °C and 55 °C at nominal point for each scenario with forced air-cooling.

C. Discussion

Each scenario has its own pros and cons, as expected in the TABLE III. Another problem that was observed in the experimental phase is the energy stored in the RF-choke (Scenario 2) that needs to be released through the shunt capacitance when driving is totally turned-off. This leads to overvoltage on the drain and possible switch breakdown. One way to overcome this issue is to gradually decrease the DC input voltage. The voltage stress on the switch is exacerbated by the non-linearity of the transistor output capacitance as shown in **Fig. 14** a) and b) for the scenarii 1 and 2. Higher switch voltage stress leads to the higher losses, referred to as "C_{OSS} losses" in the literature [28]. This is qualitatively verified with the measured temperature attained in the transistor. The

higher than predicted switch voltage is one current limitation of the presented design method. The impact of the stray inductance L_σ which is the parasitic inductance in series with the switch is another limitation. Its major impact is on the input power (measured at respectively 35 W, 42 W and 28 W for the three scenarii) below the expected 50 W. As shown in **Fig. 15** where a stray inductance between 0 nH and 15 nH has been considered, the simulation (even with perfect components) can predict this power drop.

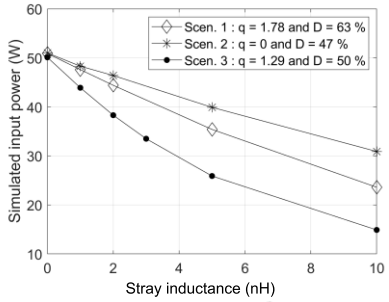


Fig. 15. Impact of the stray inductance L_σ on the class E inverter input power (simulated)

VII. Conclusion and Future Work

An in-depth analysis of the class E inverter circuit is carried out. Thanks to the normalization process, the design becomes independent to the switching frequency, the input voltage and the resistive load. A generic design method based on this analysis and an exploration of a 2-dimensional design space is presented. Three scenarii are envisioned to meet the following specifications, while ensuring optimal switching conditions: a frequency of 40.68 MHz, an output power of 50 W, a low component count, the use of a certain GaN HEMT (GS61004B) with a rated C_{OSS} and the load made of a resonant inductively-coupled WPT system. Based on that, three prototypes are implemented that reach inverter efficiencies close to 90 % thanks to the optimal switching conditions. The design method is thereby validated and should support designers along the design of VHF converters. Should the specifications be even more restrictive (e.g. a constant input current, a minimal power density or a design independent to the load variations), the design method offers to find and then compare operating points.

The limitations previously discussed should be further investigated. The applicability of the method to the design of VHF rectifiers for DC-DC power conversion is part of the future work as well.

Appendix

TABLE V
Normalized Circuit Parameters of the Class E Inverter

Parameters	
g_x, p, ϕ, k_1, k_2, V_X, V_R, $\tilde{I}_{inAC}$	Given in the appendix
Passive components	
$\tilde{L}_p$	$p/(2g_x)$
$\tilde{C}_p$	$2g_x/(q^2p)$
$\tilde{X}$	V_X/V_R
Power, input DC resistance and currents	
$\tilde{P}$	$2g_x^2$
$\tilde{R}_{DC}$	$1/(2g_x^2)$
V_{out}	$2g_x$
$\tilde{I}_r$	$2g_x$
$\tilde{I}_{in}$	$2g_x^2$
Current waveforms	
$\tilde{\imath}_r(\theta)$	$2g_x \sin(\theta+\phi)$
$\tilde{\imath}_{in}(\theta)$ *ON*	$2g_x\left(\frac{\theta}{p}-\sin(\phi)\right)$
$\tilde{\imath}_{in}(\theta)$ *OFF*	$\frac{2g_x}{p}\left(-\frac{k_1}{q}\sin(q\theta)+\frac{k_2}{q}\cos(q\theta)-\frac{q^2p}{q^2-1}\sin(\theta+\phi)\right)$
$\tilde{\imath}_s(\theta)$ *ON*	$\frac{2g_x}{p}\left(\theta+\frac{\sin(\theta+\phi)-\sin(\phi)}{p}\right)$
$\tilde{\imath}_c(\theta)$ *OFF*	$\frac{2g_x}{p}\left(-\frac{k_1}{q}\sin(q\theta)+\frac{k_2}{q}\cos(q\theta)-\frac{p}{q^2-1}\sin(\theta+\phi)\right)$
Voltage waveforms	
$\tilde{v}_s(\theta)$ *OFF*	$1+k_1\cos(q\theta)+k_2\sin(q\theta)+\frac{q^2p}{q^2-1}\cos(\theta+\phi)$
$\tilde{v}_{s1}(\theta)$	$V_R\sin(\theta+\phi)+V_X\cos(\theta+\phi)$
$\tilde{v}_{out}(\theta)$	$-2g_x\sin(\theta+\phi)$
Switch current and voltage stress	
$\tilde{V}_{sp}$	$(1.7613+0.05q)/(1-D)$
$\tilde{I}_{sp}$	(23)-(24)
c_p	$\frac{2g_x^2}{\tilde{V}_{sp}\tilde{I}_{sp}}$
Relative losses in the inductors	
ρ_{L0}	Q/Q_1
ρ_{Lp}	$\frac{p\tilde{I}_{inAC}^2}{4g_x^3Q_1}$

Expressions for parameters of TABLE V are given here.
The parameter p and the angle ϕ:

$p=\sqrt{A^2+B^2}$

$\phi=\text{atan}(A,B)$

where atan (Y, X) is the four-quadrant arctangent

$A=\frac{b_1c_2-b_2c_1}{a_2b_1-a_1b_2}$

$B=\frac{a_1c_2-b_2c_1}{a_2b_1-a_1b_2}$

$a_1=\frac{q}{q^2-1}\left(\cos\left(2\pi q(D-1)\right)-q^2\cos(2\pi D)\right)+q$

$a_2=\frac{q}{q^2-1}\left(\sin\left(2\pi q(D-1)\right)-q\sin(2\pi D)\right)$

$b_1=\frac{q}{q^2-1}\left(-q\sin\left(2\pi q(D-1)\right)+q^2\sin(2\pi D)\right)$

$b_2=\frac{q}{q^2-1}\left(q\cos\left(2\pi q(D-1)\right)-q\cos(2\pi D)\right)$

$c_1=2\pi qD-\sin\left(2\pi q(D-1)\right)$

$c_2=\cos\left(2\pi q(D-1)\right)-1$

The constant parameters k_1, k_2 and g_x:

$k_1=\frac{pq}{1-q^2}(q\cos(2\pi q)\cos\phi+\sin(2\pi q)\sin\phi)-\cos(2\pi q)$

$k_2=\frac{pq}{1-q^2}(q\sin(2\pi q)\cos\phi-\cos(2\pi q)\sin\phi)-\sin(2\pi q)$

$g_x=\frac{1}{2\pi I_r}\int_0^{2\pi}i_s(\theta)d\theta=\frac{\pi D^2}{p}-D\sin\phi+\frac{\cos\phi}{2\pi}-\frac{\cos(2\pi D+\phi)}{2\pi}$

The coefficients V_R and V_X:

$V_R=\frac{V_{in}}{\pi}\left(\frac{k_1r_1+k_2r_2+pr_3}{q^2-1}+r_4\right)$ with:

$$r_1 = -\cos(2\pi qD)\cos(2\pi D+\phi)+\cos(2\pi q)\cos\phi - q\sin(2\pi q\ D)\sin(2\pi D+\phi)+q\sin(2\pi q)\sin\phi$$

$$r_2 = -\sin(2\pi qD)\cos(2\pi D+\phi)+\sin(2\pi q)\cos\phi + q\cos(2\pi qD)\sin(2\pi D+\phi)-q\cos(2\pi q)\sin\phi$$

$$r_3 = \frac{q^2}{4}(\cos(4\pi D+2\phi)-\cos(2\phi))$$

$$r_4 = \cos(2\pi D+\phi)-\cos\phi$$

$$V_X = \frac{V_{in}}{\pi}\left(\frac{k_1x_1+k_2x_2+px_3}{q^2-1}+x_4\right) \text{ with:}$$

$$x_1 = \cos(2\pi qD)\sin(2\pi D+\phi)-\cos(2\pi q)\sin\phi - q\sin(2\pi q\ D)\cos(2\pi D+\phi)+q\sin(2\pi q)\cos\phi$$

$$x_2 = \sin(2\pi qD)\sin(2\pi D+\phi)-\sin(2\pi q)\sin\phi + q\cos(2\pi qD)\cos(2\pi D+\phi)-q\cos(2\pi q)\cos\phi$$

$$x_3 = \frac{q^2}{4}(4\pi(1-D)-\sin(4\pi D+2\phi)+\sin(2\phi))$$

$$x_4 = -\sin(2\pi D+\phi)+\sin\phi$$

The normalized AC content of the input current $\tilde{I}_{inAC}$:

$$\tilde{I}_{inAC} = \sqrt{\tilde{I}_{inRMS}{}^2-\tilde{I}_{in}{}^2}$$

where the $\tilde{I}_{inRMS}$ expression is analytically derived:

$$\tilde{I}_{inRMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\tilde{\imath}_{in}^2(\theta)d\theta} = \frac{2g_x}{p}\sqrt{\gamma_1+\gamma_2+\gamma_3+\gamma_4+\gamma_5+\gamma_6+\gamma_7}$$

$$\gamma_1 = \frac{4}{3}\pi^2D^3-2\pi D^2p\sin(\phi)-Dp^2\sin^2(\phi)$$

$$\gamma_2 = \frac{1}{2\pi}\left(\frac{k_1}{q}\right)^2\left(\pi(1-D)+\frac{1}{4q}\sin(4\pi qD)-\sin(4\pi q)\right)$$

$$\gamma_3 = \frac{1}{2\pi}\left(\frac{k_2}{q}\right)^2\left(\pi(1-D)+\frac{1}{4q}\sin(4\pi q)-\sin(4\pi qD)\right)$$

$$\gamma_4 = \frac{1}{2\pi}\left(\frac{pq^2}{q^2-1}\right)^2\left(\pi(1-D)+\frac{1}{4}\sin(4\pi D+2\phi)-\sin(2\phi)\right)$$

$$\gamma_5 = \frac{k_1k_2}{4\pi q^3}(\cos(4\pi q)-\cos(4\pi qD))$$

$$\gamma_6 = \frac{k_1pq}{\pi(q^2-1)^2}(-\sin(2\pi qD)\cos(2\pi D+\phi)+\sin(2\pi q)\cos(\phi) - q\cos(2\pi q)\sin(\phi)+q\cos(2\pi qD)\sin(2\pi D+\phi))$$

$$\gamma_7 = \frac{k_2pq}{\pi(q^2-1)^2}(\cos(2\pi qD)\cos(2\pi D+\phi)-\cos(2\pi q)\cos(\phi) - q\sin(2\pi q)\sin(\phi)+q\sin(2\pi qD)\sin(2\pi D+\phi))$$

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